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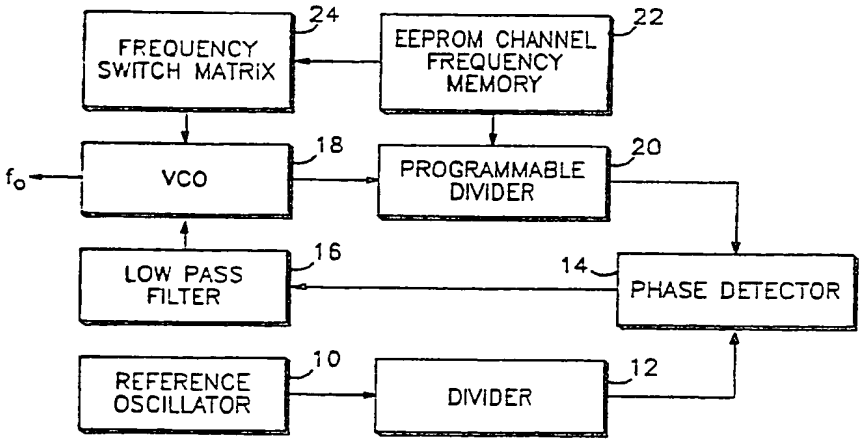
(54) Title: LOW VOLTAGE AND LOW POWER FREQUENCY SYNTHESIZER



(57) Abstract

A low power and low voltage frequency synthesizer includes a memory (22) containing information to provide divisor information to the variable divider (20) of a phase locked loop and information to select predetermined values of capacitance to connect to the frequency determining resonant network of the VCO (18) to provide a coarse tuning. This tuning is then further modified by the normal operation of the phase locked loop.

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LOW VOLTAGE AND LOW POWER FREQUENCY SYNTHESIZER

FIELD OF THE INVENTION

The field of the invention relates to frequency synthesizers for use in communication devices and more particularly, to frequency synthesizers which operate on very low voltages and reduced power.

BACKGROUND OF THE INVENTION

Frequency synthesizer phase locked loops have been utilized in communication transceivers for some period of time. The normal approach is to use a varactor tuned voltage controlled oscillator in combination with controlled modulus frequency divisors in the phase locked loop to produce the desired output frequency. In these prior art techniques, a varactor, or voltage controlled capacitor, is commonly used to vary the resonant frequency of the VCO tuning network in accordance with a control voltage. This approach requires the use of high varactor control voltages, typically, 12 volts or more, to achieve the VCO tuning range that is needed for feedback transceiver applications. In the case of small portable devices, especially single cell receivers, the voltage required and power consumed by this varactor tuning approach in a frequency synthesizer would consume excessive power and would result in a very shortened battery life.

The present invention is intended to overcome this disadvantage of the prior art by providing a channel frequency memory which provides not only the

appropriate phase locked loop divisors for a PLL-VCO synthesizer but also alters the VCO frequency tuning network by selectively adding discrete capacitors to the frequency determining network of the VCO as a course frequency adjustment. Thus, only a low voltage, low varactor network with a much reduced tuning range is required to fine tune the VCO and allow the loop to operate properly.

SUMMARY OF THE INVENTION

It is an object of the invention to provide a low voltage, low powered frequency synthesizer which is capable of operating on at most a two cell battery.

It is a further object of the invention to provide a very low power frequency synthesizer utilizing a VCO that is tuned by a combination of additive capacitors and a low voltage varactor network to cover a broad range of frequencies.

It is yet a further object of the invention to provide a phase locked loop frequency synthesizer which does not require multi-cell batteries in conjunction with voltage multipliers to achieve reasonable tuning ranges.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a block diagram of a frequency synthesizer in employing the present invention.

FIG. 2 is an additional detailed block diagram of a portion of the frequency synthesizer shown in FIG. 1.

DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 1 shows a phase locked loop frequency synthesizer, which includes many parts common with the frequency synthesizers of the prior art, but also includes additional devices as taught by the present invention. Reference oscillator 10 provides a fixed frequency reference signal to a divider 12. The divided down frequency from divider 12 is provided as a first input to phase detector 14 which provides a signal through a low pass filter 16 as a first input of VCO 18. One output of VCO 18 is connected through a programmable divider 20 and back to a second input to phase detector 14. A memory 22, for the preferred embodiment, an electrically erasable programmable read only memory containing channel frequency divisor information, modifies programmable divider 20 to adjust the division ratio of the two signals incoming to phase detector 14 so that the VCO produces an output of F_0 that is appropriate for the desired frequency synthesizer output. The operation of the elements as presently described, is well known in the art as a normal phase locked loop frequency synthesizer.

Channel frequency memory 22 not only includes division information supplied to the programmable divider 20 to adjust the output frequency, but it further includes information supplied to a frequency switch matrix 24 which adds discrete capacitors directly into the frequency determining resonant network of VCO 18. Thus, instead of requiring the high voltages and high current drains that are needed to drive the voltage controlled reactive elements used in prior art VCO tuning networks, fixed capacitance values can be selectively added to the frequency determining resonant network to

provide the appropriate range of frequency outputs that are necessary to provide a broadband frequency synthesis. This is achieved while conserving the normal power that would be required to achieve that tuning.

FIG. 2 shows, in a more detailed manner, the structure of frequency matrix 24. The channel frequency data corresponding to the desired frequency and divisor information which is supplied to divider 20 from EEPROM memory 22 is supplied to a frequency to capacitance decoding logic block 26. This frequency to capacitance decoding logic supplies an output to selector switch driver logic 28 which selects various combinations of discrete capacitance from a capacitor array 30. These values are then added to the frequency determining resonant network of VCO 18. The output of capacitor array 30 may be one or any combination up to and including all of the capacitance. When added to the frequency determining circuit this achieves a course value of tuning for the frequency determining resonant circuit of VCO 18.

In operation, the frequency to capacitance decoding logic interprets from a predetermined value the appropriate capacitance which must be added to the VCO to enable the VCO to tune in a low power vernier manner to achieve the resultant frequency F_0. The selector switch driver logic responds to the frequency to capacitance decoding logic to merely select and latch which capacitors in the capacitor array 30 must be coupled into the circuit to achieve the course tuning.

Thus, it may be seen that for various frequencies, rather than tuning the VCO with a high voltage varactor network and correspondingly

consuming the power required to maintain it and combining that with an appropriate divisor in programmable divider 20, the present low power frequency synthesizer augments the tuning capability of the VCO circuit as it is driven by an outside voltage source with discrete capacitor values to alter the tuning. The normal phase locked loop in combination with the altered coarse tuning provides the appropriate programmable frequency control ratio so that the synthesizer may provide the final output frequency F_0 in the appropriate range for desired operation. It will be clear to those skilled in the art that the switching in of the capacitor array requires considerably less power than the power required to drive the frequency determining resonant circuit of a VCO and maintain it at a fixed voltage and frequency output position for considerable lengths of time. Thus, it may be seen that the entire operation of the frequency synthesizer occurs with considerably less power consumed and may be operated with considerable lower voltages.

What is claimed is:

Claims

1. A low voltage and low power frequency synthesizer including a memory containing divisor information, a variable divider phase locked loop responsive to the divisor information for controlling the output frequency of a voltage controlled oscillator comprising:

memory means (22) containing information corresponding to the desired frequency and divisor information of the VCO; and

frequency capacitance switch means (24) coupled between said memory and said VCO responsive to additional information to select a predetermined value of capacitance, said switch means further including means producing a coarse tuning frequency by augmenting the value of capacitance in the frequency determining network of the VCO, whereby a broad range of frequencies can be synthesized at lower voltages and maintained with lower power consumption with the phase locked loop operating to maintain the precision of the desired frequency.

2. The frequency synthesizer of claim 1, wherein the memory means further comprises a programmable Read Only Memory (ROM).

3. The frequency synthesizer of claim 2, wherein said EROM is electrically erasable.

4. The frequency synthesizer of claim 1, further including a plurality of capacitors (30) from which the frequency capacitance switch means may select.

5. The frequency synthesizer of claim 4, wherein the plurality of capacitance (30) includes at least five values in a binary related sequence.

FIG. 1

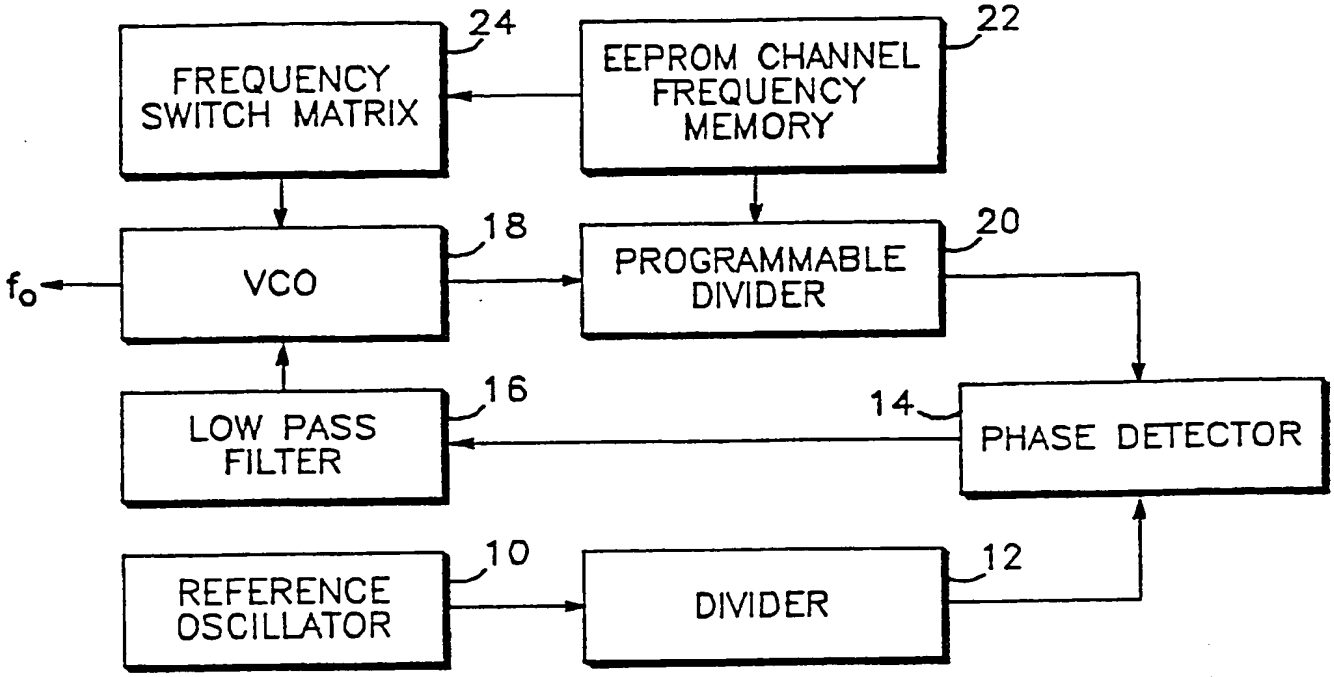
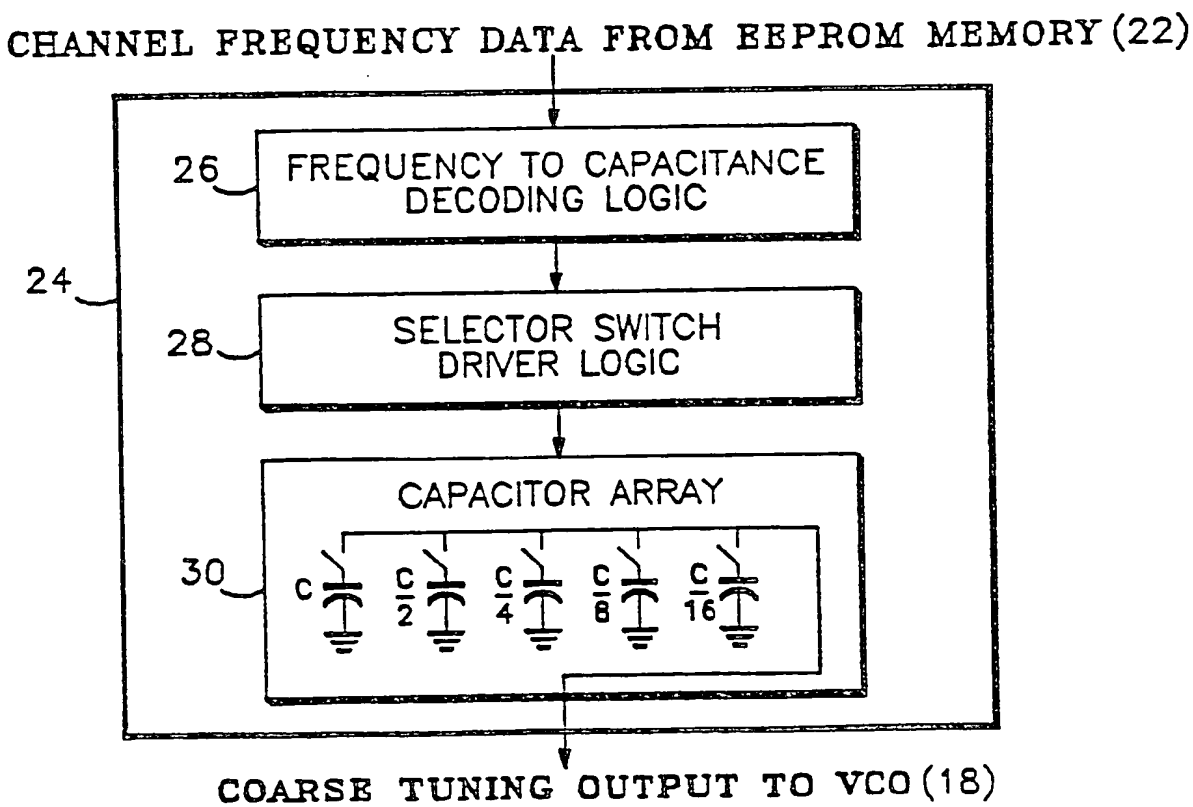


FIG. 2



INTERNATIONAL SEARCH REPORT

International Application No. PCT/US88/04547

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC (4): H03B 19/00; H03L 7/00
US CL: 307/271; 328/14,155; 331/1A

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
US	328/14,15,155 307/262,271 331/1A,16,17,18

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category *	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
A	US, A, 4,613,826 (Masuko et al) 23 September 1986.	1-5
A	US, A, 4,453,136 (Kelland) 05 June 1984.	1-5
A	US, A, 4,330,758 (Swisher et al) 18 May 1982	1-5
A	US, A, 4,305,045 (Metz et al) 08 December 1981	1-5

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IV. CERTIFICATION

Date of the Actual Completion of the International Search

28 March 1989

Date of Mailing of this International Search Report

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International Searching Authority

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Signature of Authorized Officer

Timothy P. Callahan

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